

FORM PTO-1449 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			ATTY. DOCKET NO. TI-28234	SERIAL NO.	
LIST OF DOCUMENTS CITED BY APPLICANT <i>(Use several sheets if necessary)</i>					APPLICANT Jean-Louis Tardieux		
					FILING DATE October 1, 1999		GROUP

U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE (IF APPROPRIATE)
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						

FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION Yes No
SMD	BA	EP 0 649 085 A	4/19/95	Europe	G06F 9/38	—	X
	BB						
	BG						
	BD						
	BE						
	BF						
	BG						

EXAMINER <i>S. Deckter</i>	DATE CONSIDERED <i>03/04/02</i>
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)		
	CA	TI-27677, <i>A Bit Field Processor</i> , co-filed as a regular application October 1, 1999.
	CB	TI-27678, <i>Rounding Mechanisms in Processors</i> , co-filed as a regular application October 1, 1999.
	CC	TI-27679, <i>Linear Vector Computation</i> , co-filed as a regular application October 1, 1999.
	CD	TI-27680, <i>Hardware Accelerator / Acceleration for Processing Systems</i> , co-filed as a regular application October 1, 1999.
	CE	TI-27681, <i>Pipeline Protection</i> , co-filed as a regular application October 1, 1999.
	CF	TI-27682, <i>Pipelined Hardware Stack</i> , co-filed as a regular application October 1, 1999.
	CG	TI-27683, <i>A Processor With Conditional Execution of an Instruction Pair</i> , co-filed as a regular application October 1, 1999.
	CH	TI-27684, <i>A Processor With Local Instruction Looping</i> , co-filed as a regular application October 1, 1999.
	CI	TI-27685, <i>Compound Memory Access Instructions</i> , co-filed as a regular application October 1, 1999.
	CJ	TI-27686, <i>A Processor With a Computed Repeat Instruction</i> , co-filed as a regular application October 1, 1999.
	CK	TI-27688, <i>A Processor With Apparatus for Verifying Instruction Parallelism</i> , co-filed as a regular application October 1, 1999.
	CL	TI-27689, <i>Cache Miss Benchmarking</i> , co-filed as a regular application October 1, 1999.
	CM	TI-27690, <i>A Processor With Apparatus for Indexed Branch During Instruction Iteration</i> , co-filed as a regular application October 1, 1999.
	CN	TI-27691, <i>Circular Buffer Management</i> , co-filed as a regular application October 1, 1999.
	CO	TI-27700, <i>Method and Apparatus for Accessing a Memory Core Multiple Times in a Single Clock Cycle</i> , co-filed as a regular application October 1, 1999.
	CP	TI-27757, <i>Improved Multiplier Accumulator Circuits</i> , co-filed as a regular application October 1, 1999.
	CQ	TI-27758, <i>Zero Anticipation Method and Apparatus</i> , co-filed as a regular application October 1, 1999.
	CR	TI-27759, <i>Trace FIFO Management</i> , co-filed as a regular application October 1, 1999.
	CS	TI-27760, <i>Stack Pointer Management</i> , co-filed as a regular application October 1, 1999.
	CT	TI-27761, <i>Software Breakpoint in a Delay Slot</i> , co-filed as a regular application October 1, 1999.
	CU	TI-27762, <i>Cache Coherence During Emulation</i> , co-filed as a regular application October 1, 1999.
	CV	TI-27763, <i>Memory Access Using Byte Qualifiers</i> , co-filed as a regular application October 1, 1999.
	CW	TI-27764, <i>Dual Interrupt Vector Mapping</i> , co-filed as a regular application October 1, 1999.
	CX	TI-28234, <i>Pipeline Protection</i> , co-filed as a regular application October 1, 1999.
	CY	TI-28433, <i>Improvements in or Relating to Microprocessors</i> , co-filed as a regular application October 1, 1999.
SMD	CZ	Paver, N.C., et al.; <i>Register Locking in an Asynchronous Microprocessor</i> , IEEE Proc. Of the Int'l Conf. On Computer Design: VL in Computers and Processors, Cambridge, MA, Oct. 11-14, 1992, pgs. 351-355.
SMD	DA	Shimamura, K., et al.; <i>A Superscalar RISC Processor With Pseudo Vector Processing Feature</i> , IEEE Int'l Conf. On Computer Design: VLSI in Computers and Processors, Austin, Oct. 2-4, 1995, pgs. 102-109.
SMD	DB	Kogge, P.; <i>The Architecture of Pipelined Computers</i> , 1981, Hemisphere Pub. Corp., Washington, US XP002096561, pgs. 220-225.
EXAMINER S. Deckter		DATE CONSIDERED CZ-DB ONLY 03/04/02
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